circuit located between the resistive circuit and a negative voltage source is operable to selectively connect the first and second data buses, respectively, through individual resistances, to the negative voltage source; and

enabling the first termination path when the PLD is in a receive mode; and

enabling the two second termination paths when the PLD is in a transmit mode.

REMARKS

1. Claims 2, 3, 4, 5, 7, 9,12 and 13 are amended. Claims 6 and 10. With entry of this amendment, 2-5, 7-9, 11-18 will be pending. A marked-up version of the rewritten claims is attached hereto.

2. The Office Action has rejected Claims 1-2, 5-8, 10-11, and 18 under 35 U.S.C. §102, as being anticipated by U.S. Patent Number 5,781,028 (hereafter "Decuir patent") issued to Joseph C. Decuir. As the claims in question have been deleted or amended, the rejection is now moot.

The Applicants acknowledge the Office Action's statement that Claims 3-4, and 9 would be allowable if rewritten in independent form, and to include the subject matter of the rejected base claims. The aforementioned claims have been amended to comply with these requirements. The Applicants also acknowledge and appreciate the statement that Claims 14-17 are allowed.

The Office Action has also rejected Claim 12 under 35 U.S.C. §103(a), as being obvious and therefore unpatent-

able over the Decuir patent. Claim 12 has been amended to rewrite it in independent form, and to include a limitation like the one appearing in Claim 3 regarding the switch circuit being located between the resistive circuit and a negative voltage source. This is reflective of the Examiner's statement of reasons for allowance. As the amended Claim 12 is now distinguishable over the prior art, it is believed to be allowable.

Claim 13 has not been rejected. As such, the Applicants aver that it is allowable over the prior art relied upon for the same reasons stated by the Office Action in connection with Claims 3-4, 9, and 14-17.

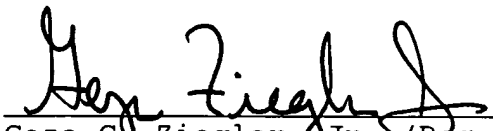
For all of the foregoing reasons, it is respectfully submitted that all of the claims now present (3, 4, 9, 12, 13, 14, 15, 16, and 17) in the application are clearly novel and patentable over the prior art of record, and are in proper form for allowance. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

A check in the amount of $920 is enclosed for a three-month extension of time.

The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit

any over payment to Deposit Account No. 16-1350.

Respectfully submitted,



Geza C. Ziegler, Jr. (Reg. No. 44,004) 6/7/02
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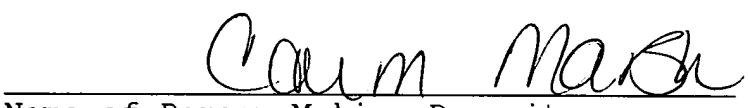
I hereby certify that the attached correspondence is being deposited with the United States Postal Service as first class mail on the date shown below in an envelope addressed to: Commissioner of Patents, Washington, DC 20231.



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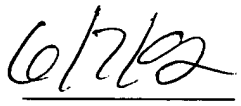

Date

Marked Up Claims

2. (Amended) A device as in claim [1] 3 wherein the differential data bus comprises a differential twisted pair line.

3. (Amended) A device [as in claim 1] for changing a termination voltage of a differential data bus, the differential data bus comprising a first data bus and a second data bus, the device comprising:

a first adjustable termination path connectable to the first data bus;

a second adjustable termination path connectable to the second data bus; and

a switch connectable in parallel with the first adjustable termination path and the second adjustable termination path;

wherein the first adjustable termination path is 50 ohm to -2 volts or 100 ohms between the first data bus and the second data bus.

4. (Amended) A device [as in claim 1] for changing a termination voltage of a differential data bus, the differential data bus comprising a first data bus and a second data bus, the device comprising:

a first adjustable termination path connectable to the first data bus;

a second adjustable termination path connectable to the second data bus; and

a switch connectable in parallel with the first ad-

justable termination path and the second adjustable termination path;

wherein the second adjustable termination path is 50 ohm to -2 volts or 100 ohms between the first data bus and the second data bus.

5. (Amended) A device as in claim [1] 3 wherein the switch is a field effect transistor (FET).

7. (Amended) A method as in claim [6] 9 wherein the step of connecting the variable termination to the differential data bus further comprises the step of:

connecting a field effect transistor (FET) to the variable termination, wherein the FET enables the first termination path or the second termination path.

8. (Amended) A method as in claim [6] 9 wherein the step of enabling the first termination path further comprises the step of configuring the first termination path to be 100 ohms between the first data bus and the second data bus.

9. (Amended) [a method as in claim 6] A method for changing terminations in an emitter coupled logic (ECL) transceiver having a differential data bus, the method comprising the steps of:

connecting a variable termination to the differential data bus, wherein the variable termination is a first termination path or two second termination paths, the differential data bus comprising a first data bus, and a second data bus;

enabling the first termination path when the ECL

transceiver is in a receive mode; and

enabling the two second termination paths when the ECL transceiver is in a transmit mode;

wherein the step of enabling the two second termination paths further comprises the steps of:

configuring a first on of the two second termination paths to be 50 ohms between the first data bus and a -2vdc source; and

configuring a second one of the two second termination [pates] paths to be 50 ohms between the second data bus and the -2vdc source.

11. (Amended) An apparatus as in claim [10] 12 wherein the variable termination further comprises :

a field effect transistor (FET), wherein the FET enables the first termination path or the second termination path.

12. (Amended) An apparatus [as in claim 10] for changing terminations in an emitter coupled logic (ECL) transceiver having a differential data bus, the apparatus comprising:

a variable termination connectable to the differential data bus, the variable termination comprising a first termination path or two second termination paths, the differential data bus having:

a first data bus connectable to the ECL transceiver; and

a second data bus connectable to the ECL transceiver;

wherein the first termination path further substan-

tially comprises 50 ohms to -2 volts or 100 ohms between the first data bus and the second data bus.

13. (Amended) An apparatus [as in claim 10] for changing terminations in an emitter coupled logic (ECL) transceiver having a differential data bus, the apparatus comprising:

a variable termination connectable to the differential data bus, the variable termination comprising a first termination path or two second termination paths, the differential data bus having:

a first data bus connectable to the ECL transceiver; and

a second data bus connectable to the ECL transceiver;

wherein the two second termination paths further [comprises] comprise:

a first one of the two second termination paths to be 50 ohms between the first data bus and a -2vdc source; and

a second one of the two second termination [pates] paths to be 50 ohms between the second data bus and the -2vdc source.

18. (Amended) At least one program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for changing terminations in a programmable logic device (PLD) having a multi-mode data bus, the method comprising the steps of:

connecting a variable termination to the multi-mode data bus, wherein the variable termination is a

first termination path or two second termination paths, the multi-mode data bus having:

a first data bus connectable to the PLD; and

a second data bus connectable to the PLD;

wherein a resistive circuit connects the first and second data buses to each other and a switch circuit located between the resistive circuit and a negative voltage source is operable to selectively connect the first and second data buses, respectively, through individual resistances, to the negative voltage source; and

enabling the first termination path when the PLD is in a receive mode; and

enabling the two second termination paths when the PLD is in a transmit mode.